4. (Twice Amended) The assembly structure recited in claim 1 wherein one of the layers of memory arrays comprises conductor line patterns.

5. (Twice Amended) The assembly structure recited in claim 1, wherein the sections forming at least one interface combine to provide a plurality of conductors.

Rule 126

~~19~~. 30 (New) An assembly structure for a memory device, comprising:

a common substrate having multiple sections;

a first layer of a memory array disposed on a first section of the multiple sections wherein the first layer of the memory array comprises a first plurality of conductor lines;

a second layer of a memory array disposed on a second section of the multiple sections wherein the second layer of the memory array comprises a second plurality of conductor lines;

at least one fold line disposed on the common substrate to define alignment of the memory arrays on the first and second sections;

wherein the sections may be folded on each other at the at least one fold line to form an operable electronic device in the memory device;

wherein at least one of the first and second layers of the memory array comprises semiconductor materials and patterns thereon to form a matrix of memory cells; and

wherein the first and second sections are folded along the at least one fold line so that the layers of the memory array are in contact with each other.